A DMOS 3A, 55V, H-Bridge: The LMD18200

Introduction

The switching power device shown in *Figure 1* is called an H-Bridge. It takes a DC supply voltage and provides 4-quadrant control to a load connected between two pairs of power switching transistors. Because the switches allow current to flow bidirectionally, the voltage across the load and the direction of current through the load can be of either polarity.

H-Bridges are often used to control the speed, position or torque of DC and stepper motors. Traditionally implemented with either discrete or monolithic bipolar transistors, fully integrated solutions are becoming increasingly popular in printer, plotter, robotics and process control applications that require 0.5A to 3.0A and operate from 12V to 55V. The LMD18200 was designed to operate within this range and was optimized for such applications.
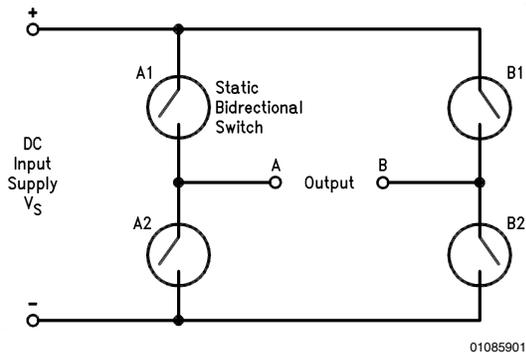

FIGURE 1. Basic H-Bridge Circuit

The LMD18200 was implemented in a process that allows bipolar, CMOS and DMOS devices to be incorporated together on one die. As each of these types of transistor structures has its own unique characteristics, each is ideally suited for a different function. By integrating them together, this allowed us to take advantage of several innovative design techniques to provide easy to use benefits typically unassociated with a simple motor driver.

Figure 2 shows a functional block diagram of the LMD18200. The circuit contains four DMOS power switching transistors, with intrinsic clamp diodes, connected in an H-Bridge configuration. All level shifting and drive circuits are included to permit control of the H-Bridge from standard logic compatible signal levels. Other unique features include current sense circuitry, overcurrent and under-voltage protection, thermal warning and thermal shutdown. Each is discussed in more detail in the following section.
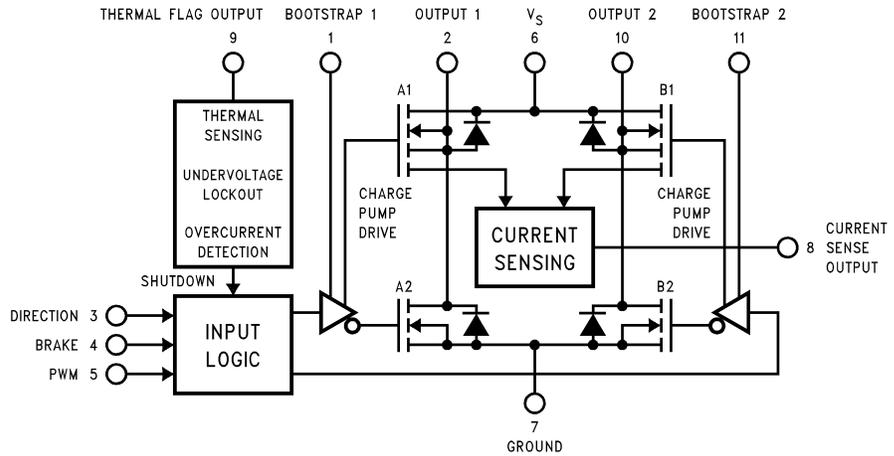
Key Features

DMOS POWER DRIVERS

DMOS power transistors allow current to flow bidirectionally and provide a lower voltage drop than similarly rated bipolar power transistors by virtue of a greatly reduced on resistance for each switch. They also have the potential to operate at much faster switching speeds for more efficient operation. And, as each switch contains its own intrinsic protection diode, the additional external protection diodes that are required for bipolar transistor implementations are no longer necessary.
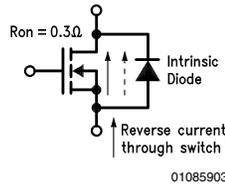
LOW ON RESISTANCE

Unlike bipolar transistors, which have a relatively high voltage drop across them, even at lower currents, the DMOS devices in the LMD18200 have a voltage drop that is essentially a linear function of temperature. The on resistance, $R_{DS(on)}$, of each output transistor is typically 0.3Ω at a junction temperature of 25˚C and 0.6Ω at 125˚C. At 100˚C and 1A of current, a comparable bipolar transistor will have a voltage drop from collector to emitter of about 1.1V whereas with the LMD18200 this voltage drop will only be 0.45V. At higher current levels the lower voltage drop across a DMOS power device provides an appreciable reduction in power dissipation resulting in smaller heat sink requirements and better efficiency with more power throughput to the load.
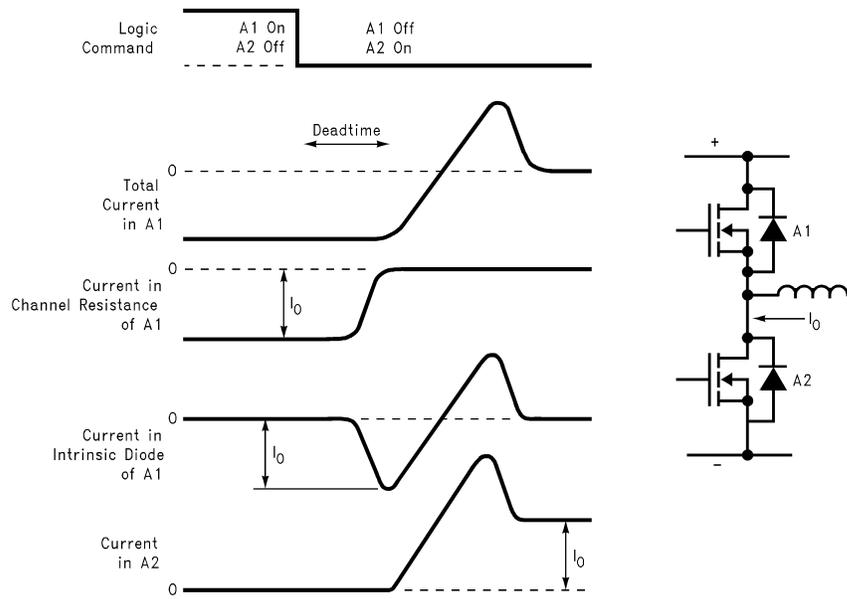
Key Features (Continued)

THERMAL FLAG OUTPUT   BOOTSTRAP 1   OUTPUT 1   V$_S$ OUTPUT 2   BOOTSTRAP 2
9   1   2   6   10   11

THERMAL
SENSING

UNDERVOLTAGE
LOCKOUT

OVERCURRENT
DETECTION

SHUTDOWN

A1   B1

CHARGE
PUMP
DRIVE

CURRENT
SENSING

CHARGE
PUMP
DRIVE

CURRENT
SENSE
8   OUTPUT

A2   B2

DIRECTION 3
BRAKE 4
PWM 5

INPUT
LOGIC

7
GROUND

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FIGURE 2. Block Diagram of the LMD18200

Ron = 0.3Ω

Intrinsic
Diode

Reverse current
through switch

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FIGURE 3. A DMOS Switch with Intrinsic Protection Diode

Logic
Command

A1 On
A2 Off

A1 Off
A2 On

Deadtime

0

Total
Current
in A1

0

Current in
Channel Resistance
of A1

I$_0$

0

Current in
Intrinsic Diode
of A1

I$_0$

Current
in A2

I$_0$

0

+

A1

I$_0$

A2

−

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**FIGURE 4. Waveforms Illustrating the Commutation of "Reverse" Current
in One Switch (A1) to "Forward" Current in Another Switch (A2)**

Key Features (Continued)

BIDIRECTIONAL CURRENT SWITCHES WITH INTRINSIC PROTECTION DIODES

When driving inductive and inertial loads such as motors the power switches must be able to conduct "forward" as well as "reverse" current. The energy stored in these types of loads must generally be free to return to the supply.

The conventional method of providing a path for reverse current is to connect an antiparallel diode across the power switch as shown in *Figure 3*.

With the DMOS structure used in the LMD18200 this diode is intrinsic. Reverse current is actually shared between the power switch and the diode due to the fact that the DMOS switch can conduct current in either direction. For current levels less than 2A to 2.5A the voltage across the power switch, ($I \times R_{DS(on)}$), is less than the forward threshold voltage of the diode and all of the current flows through the switch. At higher current levels the diode conducts and the current is shared.

An important consideration in the design of the LMD18200 was to make sure that the power switches could handle not only the load current but also the additional reverse recovery current of the protection diodes. This is illustrated in *Figure 4* where switch A1 is initially ON and conducting reverse current. At the interval when A1 is commanded OFF and the lower switch in the same leg of the H-Bridge, A2 is commanded ON, a short deadtime (purposely built in to the LMD18200 to eliminate "shoot-through" currents) occurs. During this time current begins to flow through the protection diode across switch A1. When switch A2 comes ON, the diode becomes reverse biased. Switch A2 must then conduct the load current plus the reverse recovery current of the diode for the short (approximately 100 ns) reverse recovery time of the diode. This additional requirement on the power switches has been accommodated in the design of the LMD18200.
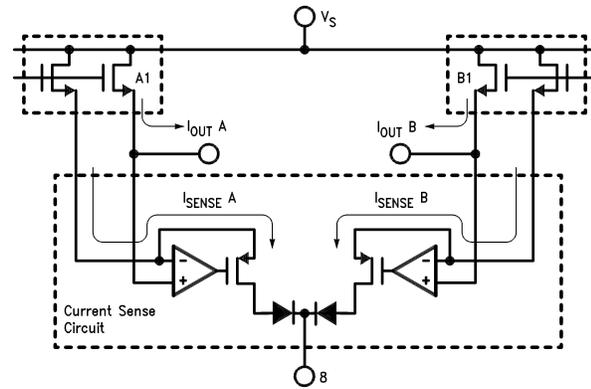
CURRENT SENSING

A unique feature of the LMD18200 is circuitry that allows for the sensing of the current through the load without affecting the supply or ground return lines. A common method for sensing the load current is to insert a small valued power resistor in series with either the V_{CC} supply or ground lines and detect the voltage drop across this resistor. This voltage drop not only takes away from the available voltage to be applied to the load but is also somewhat difficult to amplify due to very low or possibly fast varying common mode voltage presented to the amplifier.

The principle employed in the LMD18200 is the same as that used in discrete current sensing power MOSFETs. Each DMOS power transistor is actually comprised of many smaller cells connected in parallel. Due to the positive temperature coefficient of the ON resistance of each cell, the total current through the switch divides almost equally between the individual cells. A few of these cells are separated out to provide a current that is a scaled down replica of the total switch current. *Figure 5* shows a simplified functional diagram of the current sensing circuitry.

The current sourced by the Current Sense Output pin is a current proportional to the sum of the total forward current conducted by the two upper DMOS switches of the H-Bridge. This sense current has a typical value of 377 µA per Amp of current through the power devices. Simply connecting a resistor between the sense output pin and ground converts this current to a voltage proportional to the current being delivered to the load. This voltage is then suitable for feedback control or load over-current protection purposes.


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**FIGURE 5. The Current Sensing
Circuitry of the LMD18200**

CHARGE PUMP AND BOOTSTRAP CIRCUITRY

In order to drive a DMOS switch ON, its gate must be driven approximately 10V more positive than its source voltage. The lower switches of the H-Bridge have their source terminals connected to ground and their gate drive is derived from the V_S supply voltage to the device. The two upper switches however have their source terminals connected to the output pins which are continually being switched between ground and V_S. In order to generate the gate drive voltage for these switches a charge pump circuit is used. *Figure 6a* illustrates this circuitry.

Transistors Q1 and Q2 are toggled at an internally generated clock frequency of 300 kHz. When Q2 is ON, the on-chip charge pump capacitor, C_{CP}, is charged to approximately 14V. When Q1 is switched ON the bottom of this capacitor is connected to the supply voltage, V_S. This causes the voltage at point X, which connects to the gate of the upper DMOS power switch, to rise to about 14V more positive than the supply. This ensures that the upper device switches ON even if its source is at the V_S potential.

Key Features (Continued)
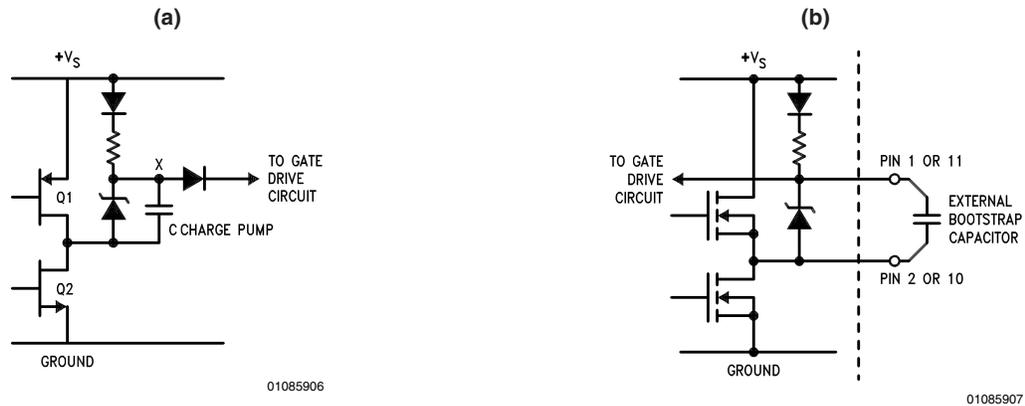
FIGURE 6. Internal Charge Pump Used in the LMD18200 (a); the Use of External Bootstrap Capacitors (b)

Capacitor C_{CP} is limited in value for practical considerations. Due to the limited charge that can be stored in C_{CP} the turn-on time of the upper DMOS transistors is relatively slow but nevertheless satisfactory for operating frequencies up to around 1 kHz. Once the DMOS device is turned ON the 300 kHz oscillator keeps the charge pump circuit running thereby holding the power device ON as long as it is commanded by the input control to do so. This charge pump circuit takes care of all the necessary voltage conditioning required by the DMOS transistors so that the external logic control applied to the LMD18200 can be simple TTL compatible signals.

For higher frequency operation, faster turn-on of the upper DMOS switches is necessary. This can be obtained through the use of external bootstrap capacitors. The bootstrap circuit is shown in *Figure 6b*. The operating principle is similar to that of the charge pump circuitry except that the switching of the bootstrap capacitor, C_B, is assumed by the DMOS power switches of the H-Bridge itself. With plenty of current available to charge these external capacitors they can have a relatively large value (10 nF is recommended) and still be charged in typically less than one microsecond. Since C_B is much larger than the input capacitance of the DMOS power transistors, these transistors can now turn ON very rapidly, typically in about 100 ns, thus allowing operating the LMD18200 at switching frequencies up to 500 kHz. *Figure 7* illustrates the switching performance of the upper transistors with and without the use of external bootstrap capacitors.
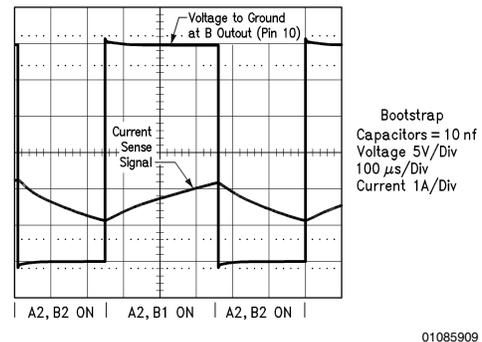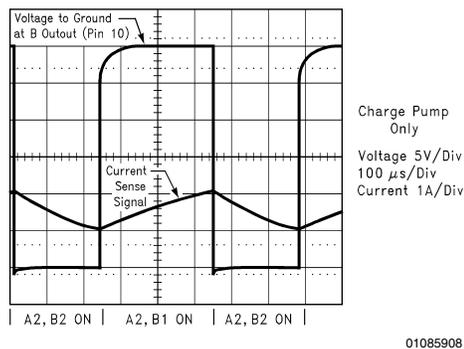
FIGURE 7. Comparison of Switching Waveforms with and without the Use of Bootstrap Capacitors

OVERCURRENT PROTECTION

The current through the upper two power DMOS switches is continually monitored and compared against a shutdown trip level (approximately 10A). In the event of a short between the two outputs or a short from either output to ground or any load condition creating excessive current to flow, the overcurrent protection circuitry will switch the upper switches OFF. A unique feature of this protection mechanism is that the protection circuitry will periodically (approximately every 8 μs) turn the upper switches back ON again, so long as the input logic is commanding the switch to be ON. This allows the H-Bridge to restart automatically following a temporary overload fault.

THERMAL WARNING/THERMAL SHUTDOWN

As with any power device protection against excessive operating temperature is a must. The LMD18200 continually senses the junction temperature near the DMOS switches and disables all of the switches in the event that this temperature reaches approximately 170˚C thus protecting the

Key Features (Continued)

device from catastrophic failure. There is a slight amount of hysteresis associated with this temperature threshold so that when the temperature cools slightly the device will automatically restart.

Another unique feature of the LMD18200 is the provision of an early warning flag of excessive operating temperature. This is an open collector output pin which pulls to a logic 0 state when the junction temperature reaches 145˚C. This flag can signal the system controller that the power driver is getting too hot and should be either shut down or have the output power cut back. The warning flags from any number of H-Bridges can be directly wired together for an "Or'd" connection.

UNDERVOLTAGE LOCKOUT

The LMD18200 also features undervoltage lockout. This circuitry disables all of the switches when the DC power supply voltage falls below approximately 10V. The reason for this feature is that reliable, well controlled operation of the switches cannot be assured without at least 10V applied.

Operation

The average output voltage across the load of the H-Bridge is continuously controlled by Pulse Width Modulation (PWM). Either polarity of output voltage can be obtained and current can flow through the load in either direction as required. The LMD18200 has three logic control inputs, PWM, Direction and Brake which control the switching action of the H-Bridge. *Figure 8* outlines the effect of these control inputs. The logic control inputs can be used directly (without external logic) to implement two of the more common PWM control techniques, Locked Antiphase control and Sign/Magnitude control.

PWM	Dir	Brake	Active Output Drivers
H	H	L	A1, B2
H	L	L	A2, B1
L	X	L	A1, B1
H	H	H	A1, B1
H	L	H	A2, B2
L	X	H	NONE

FIGURE 8. Control Logic Truth Table

LOCKED ANTI-PHASE CONTROL

The basic connection diagram and idealized waveforms for driving an inductive load using Locked Anti-phase control are illustrated in *Figure 9*. Under the control of the single PWM input signal, diametrically opposite pairs of switches (the top switch in one leg of the H-Bridge together with the bottom switch of the opposite leg) are driven ON and OFF together ("locked" together, hence the name Locked Anti-phase control). At zero average output voltage, the average voltage at each output terminal is midway between the V_{CC} supply and ground. For this condition the conduction duty cycle of each switch is 50% and the average current through the load is zero.

As the A1,B2 locked conduction interval is increased by changing the duty cycle of the control signal (75% as shown in the figure), the conduction time for the A2,B1 pair is correspondingly decreased. This duty cycle change makes the average voltage at V_OA more positive than V_OB thereby impressing a voltage across the load. The average current through the load then flows in the direction from terminal V_OA to V_OB. With a motor load this causes rotation in one direction with a speed proportional to the amount that the duty cycle deviates from 50%. Conversely, when the duty cycle is decreased to less than 50%, the average voltage from V_OA to V_OB becomes negative, the average current through the load then flows from V_OB to V_OA and the direction of rotation reverses.

If the ripple current through the load ever wants to reverse its direction it is free to do so. This is due to the fact that two switches are always driven ON and are always able to conduct current of either polarity. Another benefit of this type of control is that the voltage across the load is always defined by the state of the switches, regardless of the direction the load current wants to flow.

In applications where fast dynamic control of inertial loads (i.e., the rapid reversal of the direction of rotation of a motor) it is important that the "regeneration" of net average power from the load back to the supply be able to take place. With two switches ON there is always a path for this regenerative energy.

A major advantage of Locked Anti-phase control is that only one control signal is required to control both the speed and direction of a motor load. Simply modifying the duty cycle adjusts the average voltage and current to the load for speed control and the direction of rotation depends on whether the duty cycle is greater than or less than 50%.

One disadvantage of Locked Anti-phase control with the LMD18200 is that the current sense output is discontinuous as shown in *Figure 9*. This is because the current sensing transistors only mirror "forward" current through the upper two DMOS power devices. "Reverse" current, when the direction of current flow is in the opposite direction of what it should be for a given polarity of voltage across the load, is not output to the current sense pin.

SIGN/MAGNITUDE CONTROL

A second method of PWM control directly supported by the LMD18200 is termed Sign/Magnitude control. The ideal waveforms for this technique are illustrated in *Figure 10*.

The voltage of the output terminal of one leg of the H-Bridge is held stationary while the average voltage of the opposite leg is varied by the duty cycle of a pulse width modulated input signal. The Sign or polarity of the voltage across the load is dictated by which side of the H-Bridge is held stationary by having one of the transistors constantly ON, and the Magnitude of the average load voltage is determined by the switching duty cycle of the two switches in the opposite leg.
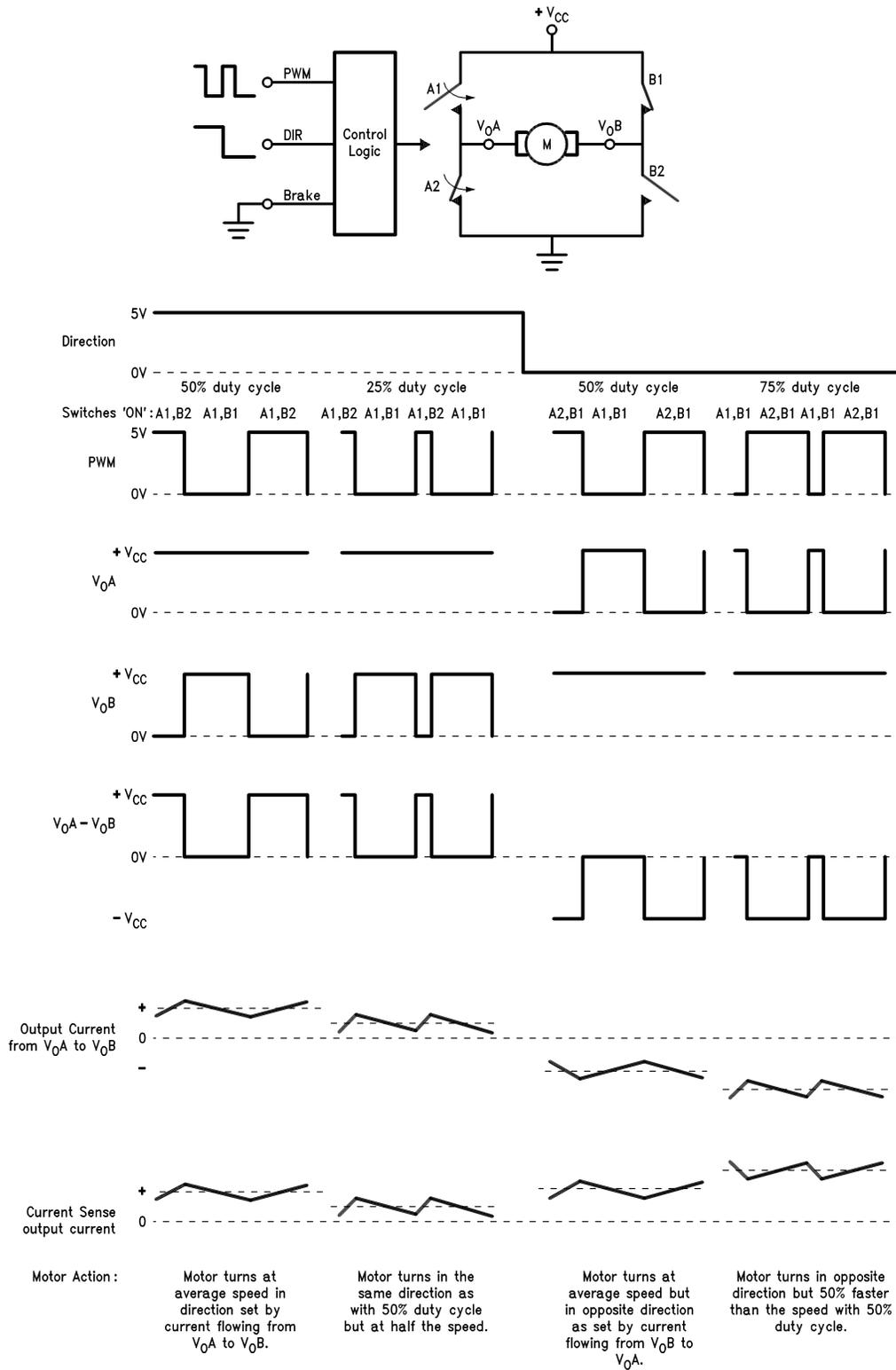
Locked Antiphase Control
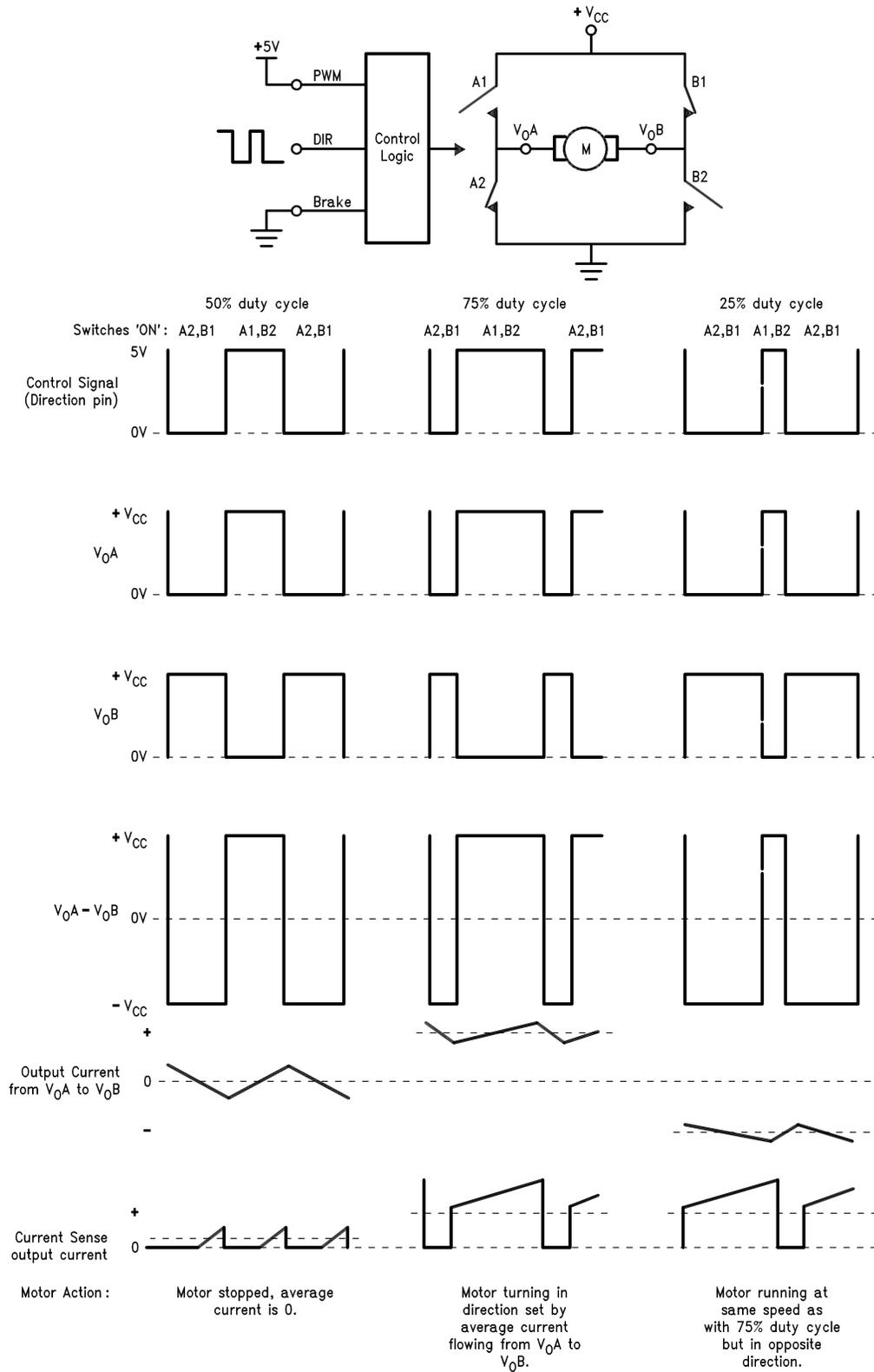
FIGURE 9. Idealized Switching Waveforms for Locked Antiphase Control

Sign/Magnitude Control

FIGURE 10. Idealized Switching Waveforms for Sign/Magnitude Control

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Sign/Magnitude Control (Continued)

The logic level applied to the Direction input turns ON either switch A1 or B1. This fixes output V_OA or V_OB at the positive supply voltage potential and therefore sets the direction of current flow through the load. The duty cycle of the signal applied to the PWM pin then adjusts the average voltage and current to the load. As the duty cycle is increased, the power to the load increases causing a faster speed of rotation of motor loads.

Keeping one of the upper transistors continually ON for Sign/Magnitude control is preferred with the LMD18200 because the current sense output will remain permanently active. Current will always be flowing through one upper transistor or the other (through switch A1 or B1) which will be sensed and output to the current sense pin. This gives a continuous representation of the load current without the discontinuities of the locked anti-phase technique. This is true so long as the direction of the current through the load corresponds with the polarity of voltage across the load. If the direction of rotation of a motor load is required to reverse there will be a short interval where the load regenerates net energy back to the supply and "reverse" current flows through the upper power devices and momentarily causes a discontinuity in the current sense output signal.

BRAKING

Emergency braking of a motor by shorting its terminals is achieved by taking both the PWM and Brake input pins to a logic 1 level. If the Direction input is at a logic 1, then braking will be accomplished by the two upper switches (A1 and B1) turning ON and shorting the motor, if a logic 0 then the lower switches (A2 and B2) will short out the motor. It is preferable to perform braking using the upper switches because they are protected by the overcurrent trip circuitry.

Calculating Power Dissipation

To obtain the full performance benefits of the LMD18200 it is important to consider the power dissipation of the device and provide adequate heat sinking as necessary. There are three components that make up the total power dissipation, Quiescent, Conductive and Switching power. The following equations will provide a worst case approximation of each of these components.

QUIESCENT POWER DISSIPATION, P_Q

This term is simply the quiescent, no load, power dissipation:

$$PQ = I_S \times V_{CC}$$

$I_S =$ the quiescent supply current (typically 13 mA with a maximum value of 25 mA)

$V_{CC} =$ the supply voltage

CONDUCTIVE POWER DISSIPATION, P_{COND}

This term is the power dissipation of the switches carrying the load current. In all applications the load current is conducted by two of the switches. The equivalent series resistance of the H-Bridge is approximately twice the on-resistance of one switch. The power dissipated by the switches can be found by:

$$P_{COND} = 2 \times I^2RMS \times R_{DS(on)}$$

$I_{RMS} =$ worst case value of the RMS load current

$R_{DS(on)} =$ the ON resistance of a power switch at the operating junction temperature, 0.33Ω typically at $25°C$ and 0.6Ω maximum at $125°C$.

SWITCHING POWER DISSIPATION, P_{SW}

Switching power dissipation is the combination of the energy dissipated by the switches and protection diodes during the ON/OFF switching action of the H-bridge. The combined total energy of a switch turning ON and the protection diode of a switch turning OFF can be approximated by:

$$E_{ON} = \frac{V_S I_O t_{ON}}{2} + V_S Q_{RR} + V_S I_O t_{RR}$$

When turning OFF one of the DMOS switches and transferring the current back to the protection diodes of the other switches, the turn-off energy can be approximated by:

$$E_{OFF} = \frac{V_S I_O t_{OFF}}{2}$$

The total average switching power dissipation can then be found by:

$$P_{SW} = (E_{ON} + E_{OFF}) \times f$$

This is the switching power dissipation for applications using Sign/Magnitude control where only one transistor is switched at a time. This power dissipation is **doubled** with locked anti-phase control because two transistors are always being switched simultaneously:

$P_{SW} = 2 \times (E_{ON} + E_{OFF}) \times f$, for locked anti-phase.

For these equations use the following values:

$V_S=$ Supply voltage

$I_O=$ peak current to the load

$t_{ON}=$ turn ON time of the DMOS transistors, 100 ns with external bootstrap capacitors, 20 µs without

$t_{OFF}=$ turn OFF time of the DMOS transistors, 100 ns with external bootstrap capacitors, 20 µs without

$Q_{RR}=$ recovered charge of the intrinsic protection diode, use 150 nanocoulombs

$t_{RR}=$ reverse recovery time of the intrinsic diode, use 100 ns

$f=$ operating switching frequency of the H-Bridge

These values will provide a good, worst case approximation of the switching power dissipation.

Total Power Dissipation, P_{TOT}

The total power dissipation of the package is the sum of these three components:

$$P_{TOT} = P_Q + P_{COND} + P_{SW}$$

At low switching frequencies, less than 50 kHz, most of the power dissipated is conductive. When operating at higher frequencies, the switching power dissipation can become considerable and must be taken into consideration.

At $25°C$ ambient operating temperature with the power TO-220 package in free air, the LMD18200 can dissipate approximately 3W without requiring a heat sink.
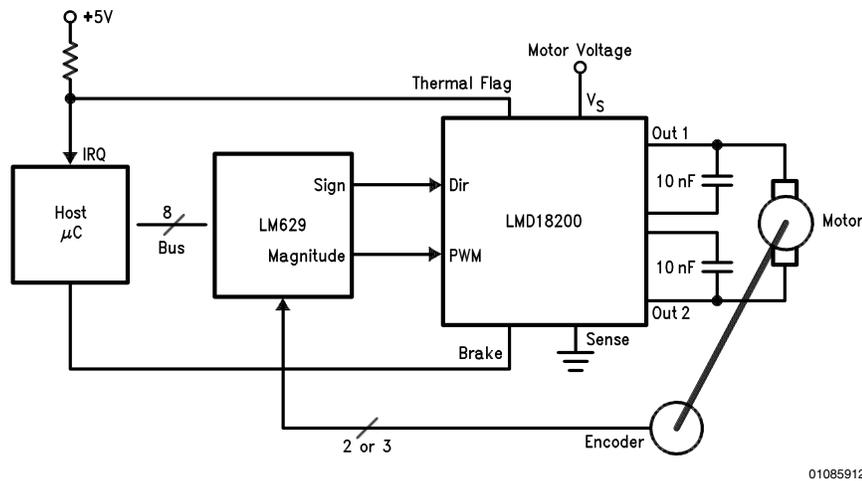
Application Examples

Applying the LMD18200 is very easy because it is fully self-contained. The only external components required for the power stage are supply bypass capacitors and optional bootstrap capacitors and/or a current sense resistor depending on the particular application. The challenging part of any application is generating and modulating the PWM control signal. This can be achieved with dedicated PWM genera-

Application Examples (Continued)

tors like the LM3524D, with simple op amp/comparator configurations, a programmable micro-controller output line, or with a dedicated motion control device like the LM629.

Figure 11 illustrates the direct interface of an LM629 to the LMD18200 to control either the position or velocity of a DC motor. The LM629 is a digitally programmable motor controller which outputs a Sign bit and variable PWM control signal to drive the LMD18200. Feedback of the motor position is accomplished via an optical shaft encoder which generates a given number of counts per revolution of the motor shaft. The digital control algorithm is processed by the LM629 in response to commands from a host microcontroller. As shown, the thermal flag output of the LMD18200 can be used to shutdown the system or back off the drive to the motor should the IC begin to overheat. Emergency braking can also be achieved by directly driving the Brake input of the LMD18200 from an output line of the processor.

In many applications it is desired to control the torque of a motor load which is proportional to the current through the motor. Using the current sense feature of the LMD18200 provides an easy means of sensing and controlling the motor current as shown in *Figure 12*. In this application the LM3524D Regulating Pulse Width Modulator compares the voltage at the current sense output pin of the LMD18200 with an externally generated control voltage and adjusts the duty cycle of the control signal (from 0 to approximately 50%) until the motor is running at the set desired current level. In this example the switching frequency is set to 40 kHz thereby requiring the use of bootstrap capacitors. This is also an example of locked anti-phase control. By simply inverting the phase of the single control input the direction of motor rotation can be reversed.

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FIGURE 11. Direct Interface of an LMD 18200 to the LM629 Motion Control Device
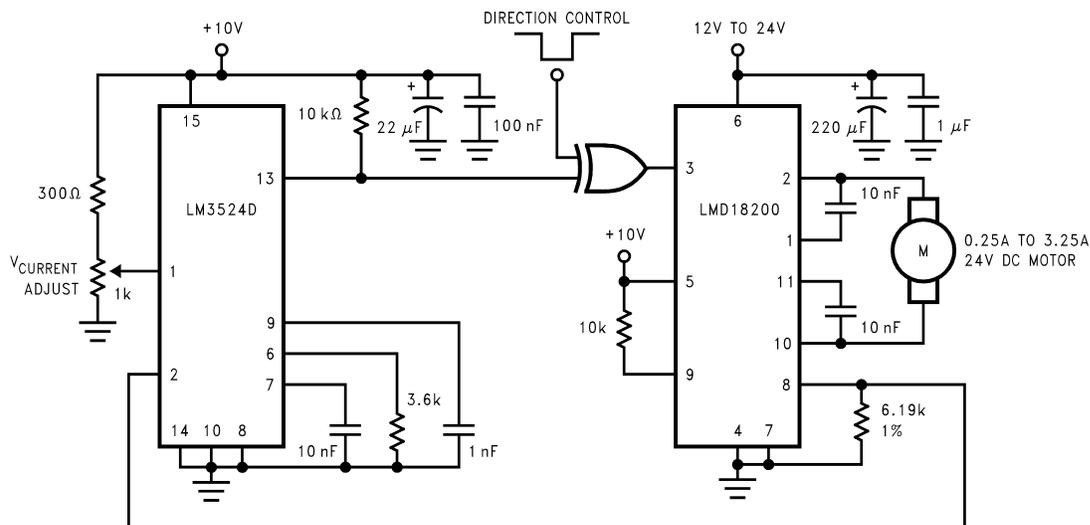
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FIGURE 12. Utilizing the Current Sense Feature to Control the Torque of a Motor Load

Application Examples (Continued)

Figure 13 shows a conventional analog control scheme termed "Fixed Off Time Control". This again takes advantage of the current sensing feature of the LMD18200. A voltage representing the current through the motor is again compared with an externally generated control voltage. Whenever the motor current exceeds the desired set level a one shot is triggered which turns on the two upper switches of the H-Bridge, shorting out the motor for a fixed time interval. This causes the motor current to decrease. At the end of the one-shot interval, voltage is reapplied to the motor until the current once again exceeds the desired level. As shown in the accompanying waveforms, *Figure 14*, the average motor current modulates or "dithers" about the preset level. The amount of ripple current is proportional to the time interval of the one-shot. A certain minimum amount of ripple is required to prevent the voltage comparator from oscillating. The equivalent of 50 mV voltage change at the input to the comparator is sufficient.
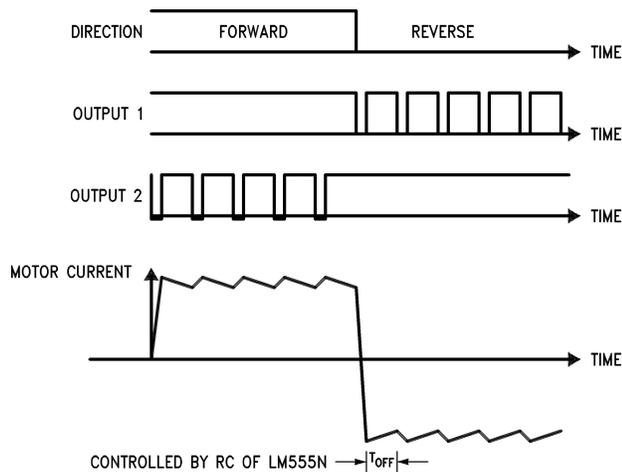
The off time interval is equal to 1.1 RC, which are the timing components for the LM555 timer.

This application is an example of Sign/Magnitude control. To reverse the motor direction simply drive the Direction input of the LMD18200.

$$T_{OFF} = 1.1\,RC$$
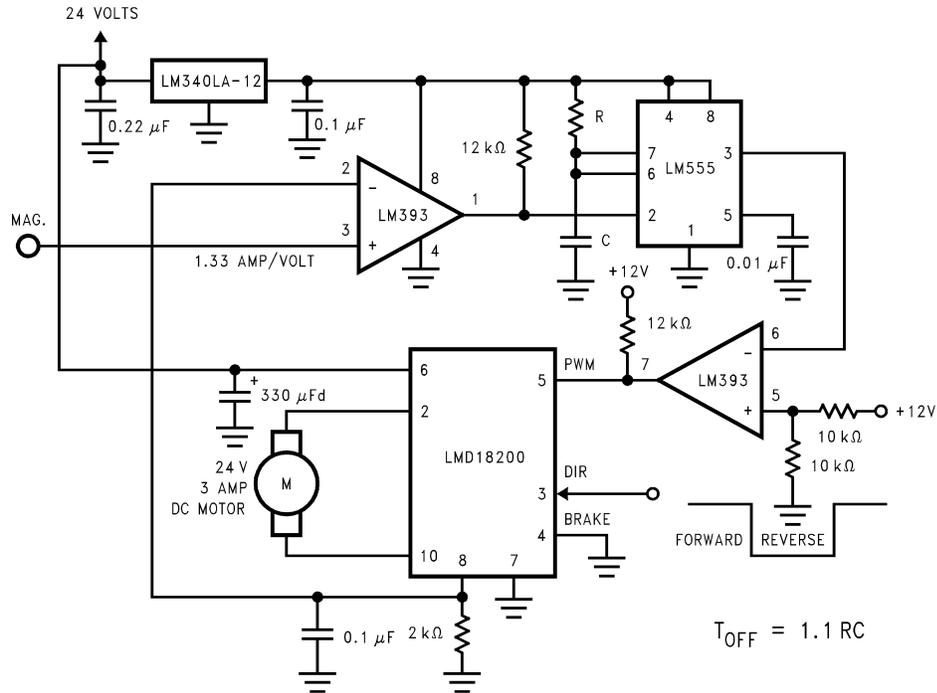
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FIGURE 13. Fixed OFF Time Control

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FIGURE 14. Switching Waveforms for the Fixed OFF Time Control Loop

Notes

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